IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:		Docket No. P27144
D. C. EDELSTEIN, *et al.*		Confirmation No. 1995
Appln. No.	: 10/707,996	Group Art Unit: 2813
Filed	: January 30, 2004	Examiner: L. M. Schillinger
For	: DEVICE AND METHODOLOGY FOR REDUCING EFFECTIVE DISLECTRIC CONSTANT IN SEMICONDUCTOR DEVICES	

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Window, Mail Stop Appeal Brief-Patents
Randolph Building
401 Dulany Street
Alexandria, VA 22314
Sir:

This appeal is from the Examiner's final rejection of claims 1-6 as set forth in the Final Office Action of January 17, 2007. A Notice of Appeal and Request for Pre-Appeal Brief Review, in response to the January 17, 2007 Final Office Action, was filed on April 17, 2007. A Panel Decision issued on July 19, 2007. The instant Appeal Brief is being timely submitted within one month of the Panel Decision, i.e., by August 20, 2007 (August 19, 2007 being a Sunday).

Payment in the amount of $ 500.00 is being concurrently submitted as payment of the requisite fee under 37 C.F.R. 41.20(b)(2). No additional fee is believed to be required for filing the instant Appeal Brief. However, if for any reason a necessary fee is required for consideration of the instant paper, authorization is hereby given to charge the fee for the Appeal Brief and any necessary extension of time fees to Deposit Account No. 09-0458.

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(I) REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation by an assignment recorded in the U.S. Patent and Trademark Office on January 30, 2004, at Reel 014296 and Frame 0430.

(II) RELATED APPEALS AND INTERFERENCES

No related appeals and/or interferences are pending.

(III) STATUS OF THE CLAIMS

Claims 1-48 are pending. Claims 7-48 stand withdrawn by the Examiner on the basis of a Restriction Requirement. Claims 1-6 stand finally rejected. Thus, finally rejected claims 1-6 are at issue in the instant appeal and form the subject matter of the instant Appeal Brief. The claims in issue are attached in the "Claims Appendix".

(IV) STATUS OF THE AMENDMENTS

A Response under 37 C.F.R.§ 1.116 was filed March 19, 2007, requesting reconsideration of the finally rejected claims. The Examiner responded with an Advisory Action mailed April 3, 2007, indicating that the Response was considered, but did not place the application in condition for allowance. Appellant submits that no amendments after final have been filed; however, all amendments to the claims have been entered.

(V) SUMMARY OF THE CLAIMED SUBJECT MATTER

The Claimed Subject Matter

INDEPENDENT CLAIM 1

With reference to page 4, line 23 (paragraph 26) to page 12, line 10 (paragraph 48) of the

instant application and to Figs 1-14, and by way of non-limiting example, the invention provides for a method of manufacturing a structure, comprising the steps of providing a structure (100) having an insulator layer (120) with at least one interconnect (130), forming a sub lithographic template mask (135 and/or 140 and/or 150) over the insulator layer (see Figs. 2 and 3), and selectively etching the insulator layer (120) through the sub lithographic template mask (135/140/150) to form sub lithographic features (160) spanning to a sidewall of the at least one interconnect (130). See page 6, line 31 (paragraph [0032]) to page 7, line 26 (paragraph [0033]).

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-4 and 6 are improperly rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,358,813 to HOLMES et al.

Whether claim 5 is improperly rejected under 35 U.S.C. § 103(a) as being Unpatenable over HOLMES alone.

(VII) A. ARGUMENT RE. 102(b) REJECTION

Claims 1-4 and 6 are improperly rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,358,813 to HOLMES, and this rejection should be withdrawn.

REJECTION OF INDEPENDENT CLAIM 1 UNDER 35 U.S.C. § 102 IS IN ERROR

The rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,358,813 to HOLMES is in error, the decision of the Examiner to reject this claim should be reversed, and the application should be remanded to the Examiner.

Independent claim 1 recites, *inter alia,*

> ... selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect.

Appellant submits that HOLMES does not disclose or even suggest at least these features.

Appellant acknowledges that, e.g., Figs. 4 and 5 of HOLMES disclose a wiring structure which has a mask layer 8 and a conductive fill 7. However, while it is apparent from Fig. 5 that the layer 8 has openings which allow etching of material underneath, the material etched in HOLMES is the conductive fill 7 and not an underlying insulator layer 2a.

Appellant emphasizes that whereas the invention provides for selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect, HOLMES specifically discloses at col. 3, lines 11-13 that "the pattern only etches into the electrode material 7 and has no effect upon the surrounding silicon oxide layer 2a" (emphasis added).

Furthermore, while the Examiner maintains that Fig. 15 of HOLMES specifically shows selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect, the Examiner has failed to appreciate that the embodiment shown in Fig. 15, like the embodiment shown in Fig. 6, utilizes an SiNit layer 5 which is described on col. 2, lines 51-53 as a "polish stop layer 5" that "prevents subsequent operations from diminishing the thickness of the upper oxide layer 2a." Thus, the embodiment shown in Fig. 15, like the embodiment shown in Fig. 6, utilizes a pattern that "only etches into the electrode material 7 and has no effect upon the surrounding silicon oxide layer 2a" (emphasis added). See col. 3, lines 11-13.

Still further, to the extent that the Examiner is relying on a comparison between Figs. 14 and 15 of HOLMES which appear to show (on the right side of the electrode material) some removal of the stop layer 5 and upper oxide layer 2a, Appellant emphasizes that HOLMES does not specifically indicate that the drawings are to scale and clearly does not show any removal of the stop layer 5 and upper oxide layer 2a on the left side of the electrode material, which would be expected if HOLMES did in fact teach to form openings in the insulating layer 2a and not just in the electrode material.

In this regard, Appellant directs the Examiner to MPEP 2125 which states:

> When the reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value. See *Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956, 55 USPQ2d 1487, 1491 (Fed. Cir. 2000) (The disclosure gave no indication that the drawings were drawn to scale. "[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue."). However, the description of the article pictured can be relied on, in combination with the drawings, for what they would reasonably teach one of ordinary skill in the art. *In re Wright*, 569 F.2d 1124, 193 USPQ 332 (CCPA 1977) ("We disagree with the Solicitor's conclusion, reached by a comparison of the relative dimensions of appellant's and *Bauer's* drawing figures, that *Bauer* 'clearly points to the use of a chime length of roughly 1/2 to 1 inch for a whiskey barrel.' This ignores the fact that *Bauer* does not disclose that his drawings are to scale. ... However, we agree with the Solicitor that *Bauer's* teaching that whiskey losses are influenced by the distance the liquor needs to 'traverse the pores of the wood' (albeit in reference to the thickness of the barrelhead)" would have suggested the desirability of an increased chime length to one of ordinary skill in the art bent on further reducing whiskey losses." 569 F.2d at 1127, 193 USPQ at 335-36.)

At the very least, the Examiner must acknowledge that the specification of HOLMES is entirely silent with regard to etching any part of the silicon oxide layer 2a and only discloses etching into the electrode material 7 (see col. 3, lines 11-13).

In the Advisory Action of April 3, 2007, the Examiner emphasizes that Figs. 4-6 of HOLMES disclose forming a sub lithographic template mask over the insulator layer and selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect.

Appellant disagrees. It is not disputed that Fig. 4 shows a silicon nitride hard mask 8 arranged over a silicon nitride stop layer 5, that the layer 8 is arranged over electrode 7, and that layer 5 is arranged over oxide 2a. Nor is it disputed that Fig. 6 shows that the layers 8 and 5 are removed by etching and that valleys 10a are formed by etching into the electrode 7 (see col. 3, lines 1-17). However, this is simply not the same as selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect. First, although the Examiner argues that the silicon nitride stop layer 5 of HOLMES is properly interpreted as the recited insulator layer, the Examiner has failed to identify any language in HOLMES which supports the Examiner's position that the layer 5 is in fact an insulator layer. Nor has the Examiner identified any prior art document which explains that a silicon nitride stop layer 5 is *per se* an insulator layer. Second, because HOLMES discloses that both layers 8 and 5 are etched away (see col. 3, lines 16-17 and Fig. 6), it is not apparent that HOLMES teaches to selectively etch layer 5, which the Examiner has identified as the recited insulator layer. Third, because HOLMES etches both the silicon nitride hard mask 8 and the silicon nitride stop layer 5 during the formation of the valleys 10a in electrode 7, it is not understood how HOLMES can be properly interpreted to disclose selectively

etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect. The reasons are threefold:

First, as is apparent from Fig. 6, the layer 5 is clearly not etched through the layer 8 to form the features 10a. Instead, the features 10a are formed in electrode 7 by etching through layer 8. The etching of the layer 5 does not participate in forming the features 10a, which are only formed in the interconnect 7 below layer 8 and in areas not covered by layer 5.

Second, col. 3, lines 11-16 of HOLMES specifically makes clear that the so-called lithographic features 10a are formed by etching "only .. into the electrode material 7" (emphasis added). In HOLMES, no features are formed by etching an insulator layer, much less, by etching layer 5. In fact, layer 5 is a stop layer, which would prevent etching therethrough. Again, features 10a are only formed in the electrode 7 by etching layer 8.

Third, a proper interpreted claim 1 requires etching of the insulator layer through the sub lithographic template mask to form sub lithographic features in the insulator layer. Otherwise, the Examiner is ignoring the language of claim 1 which clearly recites that the insulator layer is provided with at least one interconnect, and that the sub lithographic features are formed so that they span to a sidewall of the at least one interconnect. In contrast, a fair comparison of Figs. 4-6 of HOLMES clearly shows that the features 10a are formed in the electrode 7, not in the so-called "insulator" layer 5 (i.e., a stop layer). As no features are formed in layer 5 (or layer 2a for that matter), the features 10a cannot span to a sidewall of the at least one interconnect 7. Thus, in HOLMES, the features 10a are only formed in electrode 7 by virtue of etching layer 8, and are not formed in layer 5 by etching layer 5.

Finally, to the extent that the Examiner is basing the instant rejection on an argument of inherency consistent with MPEP § 2112, Appellant notes that MPEP § 2112 specifically states, in part:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

The Examiner has neither stated that the rejection is based on inherency, nor provided any basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.

Because the above-noted document fails to disclose, or even suggest, at least the above-noted features of the instant invention, Appellant submits that no proper reading of HOLMES renders anticipated the combination of features recited in at least independent claim 1.

REJECTION OF DEPENDENT CLAIM 2 UNDER 35 U.S.C. § 102 IS IN ERROR

The rejection of claim 2 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,358,813 to HOLMES is in error, the decision of the Examiner to reject this claim should be reversed, and the application should be remanded to the Examiner.

Claim 2 depends from claim 1 and further recites:

> wherein the sub lithographic features are substantially vertical columns in the insulator layer.

The Examiner identifies Fig. 15 of HOLMES as disclosing that the recited sub lithographic features are substantially vertical columns in the insulator layer (claim 2). Appellant disagrees.

The Examiner's rejection of claim 2 is improper for at least two reasons. First, the Examiner is basing an anticipation rejection of claim 2 on a combination of two different embodiments, i.e., the embodiment of Figs. 4-6 used to reject claim 1and the alternative embodiment of Fig. 15 (see col. 2, lines 1-2 of HOLMES). While this may be proper in an obviousness rejection, this is not proper in an anticipation rejection. Second, even accepting the Examiner's assertion that the silicon nitride stop layer 5 of HOLMES is properly characterized as the recited insulator layer, the Examiner must acknowledge that the so-called insulator layer 5 does not have any sub lithographic features, much less, ones which have the form of substantially vertical columns. Fig. 15, like Fig. 6, clearly shows that the so-called features 10a are formed in the electrode material 7, and not in the so-called insulator layer 5. Claim 2 specifically recites that the substantially vertical columns are in the insulator layer. In contrast, Fig. 15 of HOLMES shows the features 10a formed only in the electrode material 7.

Because the above-noted document fails to disclose, or even suggest, at least the above-noted features of the instant invention, Appellant submits that no proper reading of HOLMES renders anticipated the combination of features recited in at least dependent claim 2.

REJECTION OF DEPENDENT CLAIM 3 UNDER 35 U.S.C. § 102 IS IN ERROR

The rejection of claim 3 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,358,813 to HOLMES is in error, the decision of the Examiner to reject this claim should be reversed, and the application should be remanded to the Examiner.

Claim 3 depends from claim 1 and further recites:

... wherein the sub lithographic features further include a plurality of holes formed in a

capping layer beneath the sub lithographic template mask and having a diameter or cross section less than a diameter or cross section of the at least one interconnect and also substantially equal to the substantially vertical columns in the insulator layer.

The Examiner identifies Fig. 13 of HOLMES as disclosing that the sub lithographic features further include a plurality of holes formed in a capping layer beneath the sub lithographic template mask and having a diameter or cross section less than a diameter or cross section of the at least one interconnect and also substantially equal to the substantially vertical columns in the insulator layer. Appellant disagrees.

The Examiner's rejection of claim 3 is improper for at least four reasons. First, the Examiner is basing an anticipation rejection on a combination of two embodiments, i.e., the embodiment of Figs. 4-6 used to reject claim 1 and the alternative embodiment of Figs. 13 and 15 (see col. 2, lines 1-2 of HOLMES). Again, while this may possibly be proper in an obviousness rejection, this is not proper in an anticipation rejection. Second, the Examiner's assertion that Fig. 13 shows the recited capping layer is incorrect. It is true that Fig. 13 shows a silicon nitride hard mask 8 arranged over a silicon nitride stop layer 5, and that an oxide layer is arranged in the openings of the layer 8. However, to the extent that the oxide formed in the openings of layer 8 can be properly characterized as the recited capping layer, the Examiner must acknowledge that this oxide layer is clearly not beneath the sub lithographic template mask 8. Third, claim 3 requires that a plurality of holes are formed in a capping layer beneath the sub lithographic template mask. However, Fig. 13 clearly shows no features or holes formed in any layers. To the extent that layer 8 has holes, they are filled with the oxide, and vice versa. Layer 5 is also lacking in any features or holes. Fourth, Fig. 15 at most shows the features 10a formed

only in the oxide layer and the electrode material 7. However, even in Fig. 15, no features or holes are shown formed in a capping layer beneath the sub lithographic template mask. To the contrary, Fig. 15 lacks the recited mask layer 8 and has no capping layer beneath it. To the extent that the oxide layer can be called the recited capping layer, (a) it is not beneath any layer, (b) it is certainly not beneath layer 8 (which has been removed in Fig. 15), and (c) layer 5 cannot be characterized as the recited capping layer 5 at least because it is not beneath layer 8 (which has been removed) and has no holes formed therein.

Because the above-noted document fails to disclose, or even suggest, at least the above-noted features of the instant invention, Appellant submits that no proper reading of HOLMES renders anticipated the combination of features recited in at least dependent claim 3.

REJECTION OF DEPENDENT CLAIM 6 UNDER 35 U.S.C. § 102 IS IN ERROR

The rejection of claim 6 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,358,813 to HOLMES is in error, the decision of the Examiner to reject this claim should be reversed, and the application should be remanded to the Examiner.

Claim 6 depends from claim 1 and further recites:

> ... wherein the sub lithographic features are substantially vertical columns in the insulator layer; and
> the sub lithographic features further include a plurality of holes having a diameter less than a diameter of the at least one interconnect and substantially equal to the substantially vertical columns in the insulator layer and a top portion of the holes are tapered.

The Examiner identifies Fig. 10 of HOLMES as disclosing that the sub lithographic features are substantially vertical columns in the insulator layer and that the sub lithographic features further include a plurality of holes having a diameter less than a diameter of the at least

one interconnect and substantially equal to the substantially vertical columns in the insulator layer and a top portion of the holes are tapered. Appellant disagrees.

The Examiner's rejection is improper for at least two reasons. First, the Examiner's assertion that hexagon shaped holes (as shown in Fig. 10) are the same as holes whose top portions are tapered is without merit. Second, even accepting the Examiner's assertion that the silicon nitride stop layer 5 of HOLMES is properly characterized as the recited insulator layer, the Examiner must acknowledge that the so-called insulator layer 5 does not have any sub lithographic features, much less, ones which have the form of substantially vertical columns. As explained above, Fig. 6 clearly shows that the so-called features 10a are formed in the electrode material 7, and not in the so-called insulator layer 5. As claim 6 specifically recites that the substantially vertical columns are formed in the insulator layer and as Fig. 6 of HOLMES shows the features 10a formed only in the electrode material 7 (not in the layer 5), this rejection is improper.

Because the above-noted document fails to disclose, or even suggest, at least the above-noted features of the instant invention, Appellant submits that no proper reading of HOLMES renders anticipated the combination of features recited in at least dependent claim 6.

B. ARGUMENT RE. 103(a) REJECTION

Claim 5 is improperly rejected under 35 U.S.C. § 103(a) as being unpatenable over U.S. Patent No. 6,358,813 to HOLMES alone, and this rejection should be withdrawn.

REJECTION OF DEPENDENT CLAIM 22 UNDER 5 U.S.C. § 103 IS IN ERROR

The rejection of claim 5 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent

No. 6,358,813 to HOLMES alone is in error, the decision of the Examiner to reject this claim should be reversed, and the application should be remanded to the Examiner.

Claim 5 depends from claim 4 and 1 and further recites:

> ... wherein the etching step includes an isotropic etching to meld at least adjacent nano columns together and provide an undercut below the at least one interconnect.

The Examiner explains that Appellant has admitted in the specification that the features of claim 5 are known. This is incorrect for at least three reasons.

First, the Examiner has failed to point to any language in the specification which supports the Examiner's position that the features of claim 5 are admitted to be known. Second, claim 5 specifically recites that an undercut is formed below the at least one interconnect. All of the embodiments shown in HOLMES, however, show features 10a which do not extend to a position below the electrode material 7. As such, HOLMES clearly fails to disclose or suggest any undercuts formed below the at least one interconnect 7. Third, even if it were known to form undercuts beneath an interconnect, neither the specification nor HOLMES provide any reason or basis for melding together adjacent features 10a or for utilizing undercuts in the features 10a of HOLMES.

Because the above-noted document fails to disclose, or even suggest, at least the above-noted features of the instant invention, Appellant submits that no proper reading of HOLMES renders unpatentable the combination of features recited in at least dependent claim 5.

CONCLUSION

Each of claims 1-6 are patentable under 35 U.S.C. §§ 102(b) and 103(a). Accordingly, Appellant respectfully requests that the Board reverse the decision of the Examiner to reject claims 1-6 under 35 U.S.C. § 102(b and 103(a), and remand the application to the Examiner for withdrawal of the above-noted rejections. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458.

Respectfully submitted,
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Attachments:
Claims Appendix
Evidence Appendix
Related Proceedings Appendix

VIII. CLAIMS APPENDIX

1. A method of manufacturing a structure, comprising the steps of:

providing a structure having an insulator layer with at least one interconnect;

forming a sub lithographic template mask over the insulator layer; and

selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect.

2. The method of claim 1, wherein the sub lithographic features are substantially vertical columns in the insulator layer.

3. The method of claim 2, wherein the sub lithographic features further include a plurality of holes formed in a capping layer beneath the sub lithographic template mask and having a diameter or cross section less than a diameter or cross section of the at least one interconnect and also substantially equal to the substantially vertical columns in the insulator layer.

4. The method of claim 1, wherein the etching step is an anisotropic etching forming a plurality of the sub lithographic features defined as nano columns.

5. The method of claim 4, wherein the etching step includes an isotropic etching to meld at least adjacent nano columns together and provide an undercut below the at least one interconnect.

6. The method of claim 1, wherein:

the sub lithographic features are substantially vertical columns in the insulator layer;

the sub lithographic features further include a plurality of holes having a diameter less than a diameter of the at least one interconnect and substantially equal to the substantially vertical columns in the insulator layer and a top portion of the holes are tapered.

IX. EVIDENCE APPENDIX

This section lists evidence submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132, or any other evidence entered by the Examiner and relied upon by Appellant in this appeal, and provides for each piece of evidence a brief statement setting forth where in the record that evidence was entered by the Examiner. Copies of each piece of evidence are provided as required by 37 C.F.R. §41.37(c)(ix).

NO.	EVIDENCE	BRIEF STATEMENT SETTING FORTH WHERE IN THE RECORD THE EVIDENCE WAS ENTERED BY THE EXAMINER
1	N/A	N/A

X. RELATED PROCEEDINGS APPENDIX

Pursuant to 37 C.F.R. §41.37(c)(x), copies of the following decisions rendered by a court of the Board in any proceeding identified above under 37 C.F.R. §41.37(c)(1)(ii) are enclosed herewith.

NO.	TYPE OF PROCEEDING	REFERENCE NO.	DATE
1	N/A	N/A	N/A